This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

In the Specification

Please replace as-filed paragraph [0031] with the following amended paragraph [0031]:

Initially, pad oxide layer 22 and pad nitride layer 40 are deposited over the substrate and then a plurality of deep trenches 20 are formed from the top surface down into the substrate 10, preferably a silicon substrate, by known patterning and etching techniques. These deep trenches 20 are formed within the DRAM 100 array area 102 of the substrate 10. An outer buried plate in the substrate and a node dielectric (not shown) are then formed. A collar oxide 24 is formed within a middle portion of each of these deep vertical trenches 20 for preventing the formation of a parasitic transistor and then the trenches filled with polysilicon to a sufficient depth within the lower portion 20b of the deep trenches to act as the conductor for the storage node.

Please replace as-filed paragraph [0032] with the following amended paragraph [0032]:

A trench top oxide layer 22' ~~layer 22"~~ is deposited within the deep trenches and then a gate oxide is deposited in the upper portions 20a of the trenches over the trench top oxide layer 22'~~oxide 22"~~. Subsequently, these upper portions of the deep trenches are filled with additional polysilicon to a sufficient depth to serve as the gate conductors (GC) for the DRAM cell. The DRAM is provided with vertical sidewall spacers 52 within the deep

trenches 20, whereby these sidewall spacers are formed by depositing a SiN layer and etching using an anisotropic dry etch technique, such as, Reactive Ion Etch (RIE). The remaining portions of the deep trenches are completely filled with additional polysilicon and the substrate surface area is then planarized to remove any excess polysilicon fill material.

Please replace as-filed paragraph [0033] with the following amended paragraph [0033]:

Thus, as shown in Fig. 1, the trench top oxide layer 22' ~~layer 22"~~ divides the deep trenches into a vertical transistor portion residing in the upper portion 20a of the trench, above the trench top oxide layer 22'~~oxide 22"~~, and a trench capacitor portion residing in the lower portion 20b of the trench, below the trench top oxide layer 22'~~oxide 22"~~. The trench top oxide layer isolates the pass transistor from the trench capacitor by isolating the gate oxide in the upper portion of the trenches from the storage node in the lower portion of the trenches. As shown, the collar oxide 24 is located within each of the trenches 20 to a depth just below the trench top oxide layer 22'~~oxide 22"~~, i.e., below the transistor portion of deep trenches 20, so as to prevent outward leakage of charge stored within the capacitor (not shown) located in the lower portion of trenches 20.